A 1.8 V Monolithic CMOS Nested-Loop Frequency Synthesizer for GSM Receivers at 1.8 GHz

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Abstract – A low-power, integrated 1.8 GHz nested-loop frequency synthesizer for GSM at 1.8 GHz in a 0.18 µm CMOS technology is presented. The synthesizer consists of two voltage-control oscillators (VCOs) and uses band switching MIM capacitors and analog tuning circuits using pMOS capacitors. Both VCOs and loop-filters are integrated on-chip. The IF VCO phase noise is -131 dBc/Hz@600kHz from a 450 MHz carrier and the RF VCO phase noise is -121 dBc/Hz@600kHz from a 1.8 GHz carrier. The power consumption of this nested-loop frequency synthesizer is 36mW@1.8V and has a die size of 3000 µm x 2000 µm.

I. Introduction

Phase-locked loops (PLLs) are an essential part of any wireless transceiver architecture. It is mainly used as the local oscillator or frequency synthesizer [1]. Reducing the number of off-chip components, while maintaining the requirements for a given specification, such as GSM, is becoming increasingly more important for low-power, low-cost solutions.

This paper presents results of various circuit components for an integrated nested-loop PLL for GSM at 1.8 GHz in a 0.18 µm CMOS technology. Measurement results are provided for the frequency dividers and the phase-frequency detectors (PFDs). Phase noise simulation results for both the IF and RF VCOs, along with its tuning range characteristics using pMOS capacitors are given. Power consumption and performance estimations of this architecture are also provided.

II. Nested-Loop PLL Architecture

The nested-loop PLL architecture used is shown in Fig. 1 [2]. This architecture has a fixed division ratio, N_1, which is confined within an outer phase-locked loop, thus creating a nested-loop configuration. When the loop has reached steady state, the output frequency f_0, will be equal to $N_2 f_{ref}$, and the output of IF VCO will settle to f_0/N_1.

For the GSM-1800 specification, if N_1 is set to 4, the IF VCO operates in the range of 425-475 MHz. With such a frequency, the inner loop will have a very wide bandwidth, while maintaining adequate suppression of the spur at f_0/N_1.

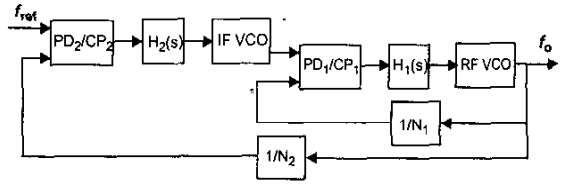

Fig. 1. Nested-loop PLL architecture

This nested-loop architecture achieves the integration of the RF VCO at the expense of an external tank for the IF VCO. However, since the IF VCO is operating at a lower frequency, it does not suffer from interference problems with the power amplifier (PA) or leakage problems, as the RF VCO does. The extra power required for the IF VCO will also be low, since it is operating at a frequency 4 times below that of the RF.

III. High Frequency Dividers

In this architecture two frequency dividers, N_1 and N_2 are required. The asynchronous divider N_1 uses 2 stages of positive edge triggered D flip-flops connected in a divide-by-two configuration.

The programmable frequency divider N_2, based on the pulse and swallow (PS counter) implementation is shown in Fig. 2 [3]. It consists of a dual-modulus $N/N+1$ prescalar, a programmable (P) counter, and a swallow (S) counter.

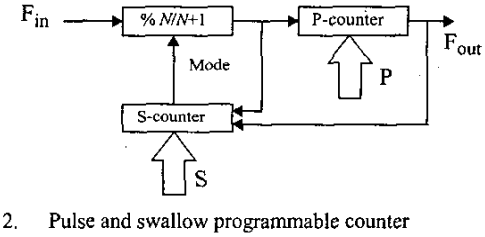

Fig. 2. Pulse and swallow programmable counter

The operation is as follows. When the mode signal is set to 0, the $N/N+1$ prescalar divides the input signal by $N+1$ for S clock cycles. Once the S counter has counted S clock cycles, the mode signal is set to 1 and the prescalar will then divide the input signal by N for the remaining P clock

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cycles. Once P clock cycles have been counted, the process repeats. This can be described by the following:

$$N_2 = (P+2)N + (S+1) \quad (1)$$

where, there are additional pulse delays of 2 and 1 in the P and S counters respectively due to the hardware implementation. Fig. 3 shows the measured results for three different combinations of P and S, all with input frequencies of 25 MHz and $N = 64$.

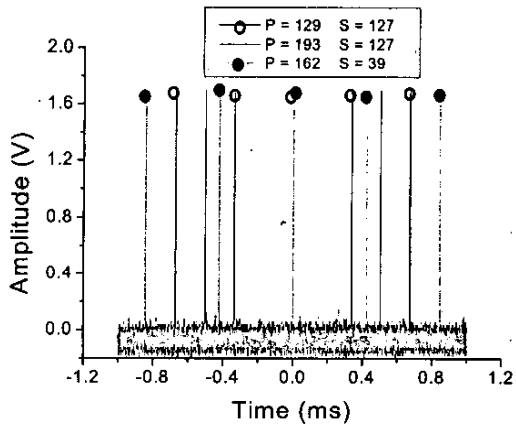

Fig. 3. Measured results of the PS Counter with input frequencies of 25 MHz. The output frequency are 2.971 kHz (P=129, S=127), 1.988 kHz (P=193, S=127) and 2.365 kHz (P=162, S=39) respectively with $N = 64$.

IV. Phase-Frequency Detector

The phase-frequency detector (PFD) shown in Fig. 4, is a conventional circuit, which consists of two D flip-flops and a NAND gate [4]. It generates UP and down (DN) pulse signals with minimum width, even when in lock, in order to eliminate the dead-zone in the phase-voltage transfer characteristic of the phase detector. This allows the loop to track small changes in the reference while still maintaining the loop in lock.

The PFD operation is as follows. When input signal REF has a rising edge before the VCO signal, an UP signal is generated in order to raise the voltage-controlled oscillator frequency. After a certain time, when the input frequency of the VCO signal sees a rising edge, a DN signal is generated in order to stop the rising of the voltage-controlled oscillator frequency. In a similar manner, if the frequency of the signal VCO is larger than that of the REF signal, the pulse width of the UP signal increases gradually in order for the frequency difference to be detected. Due to the delay of the NAND gate, both the UP and DN signals are turned on simultaneously for a short period of time.

Measurement results of the PFD with input REF and VCO signals of 5 MHz and 4 MHz respectively can be seen in Fig. 5. As can be seen, the REF signal is leading the VCO signal, thus the DN signal has finite pulse width and the UP signal is varying.

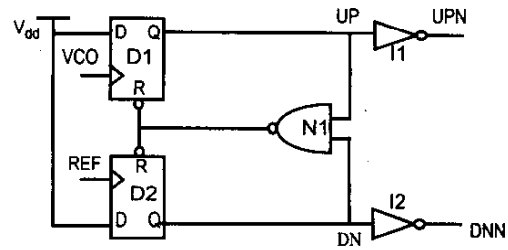

Fig. 4. The conventional phase-frequency detector

V. Charge Pump and Loop Filter

Fig. 6 shows the simplified circuit implementation of the current steering charge pump and its loop filter [5]. Using the iterative design procedure described in [6], the circuit component parameters of the loop filter and the charge pump current bias were determined. The bandwidth of the IF filter is 20 kHz with a charge pump current of 201.7 μA and that of the RF loop is 1.2 MHz with a charge pump current of 127.8 μA.

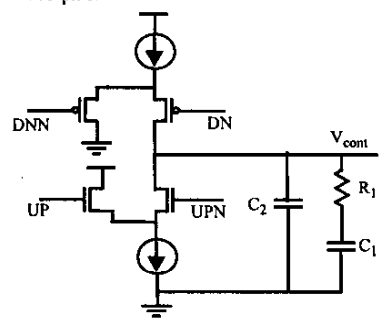

Fig. 6. Charge pump and loop filter implementation

VI. IF and RF VCOs

The IF and RF VCOs are fully integrated differential cross-coupled inductance-capacitance LC VCOs. The exception being the off chip inductors required for the IF VCO. The RF VCO tank consists of on-chip spiral inductors and uses pMOS capacitors for frequency tuning [7]. Switching capacitances are also used to switch between the mobile receive and transmit bands of GSM-1800. pMOS cross-coupled pairs were used to further reduce the $1/f$ noise [8]. Fig. 7. shows the cross-coupled LC VCO.

Fig. 8 shows the simulated phase noise performance of the IF VCO over its tuning range. As can be seen the frequency range is 422-495 MHz and has a maximum phase noise of -131 dBc/Hz at an offset of 600 kHz from a carrier of 495 MHz.

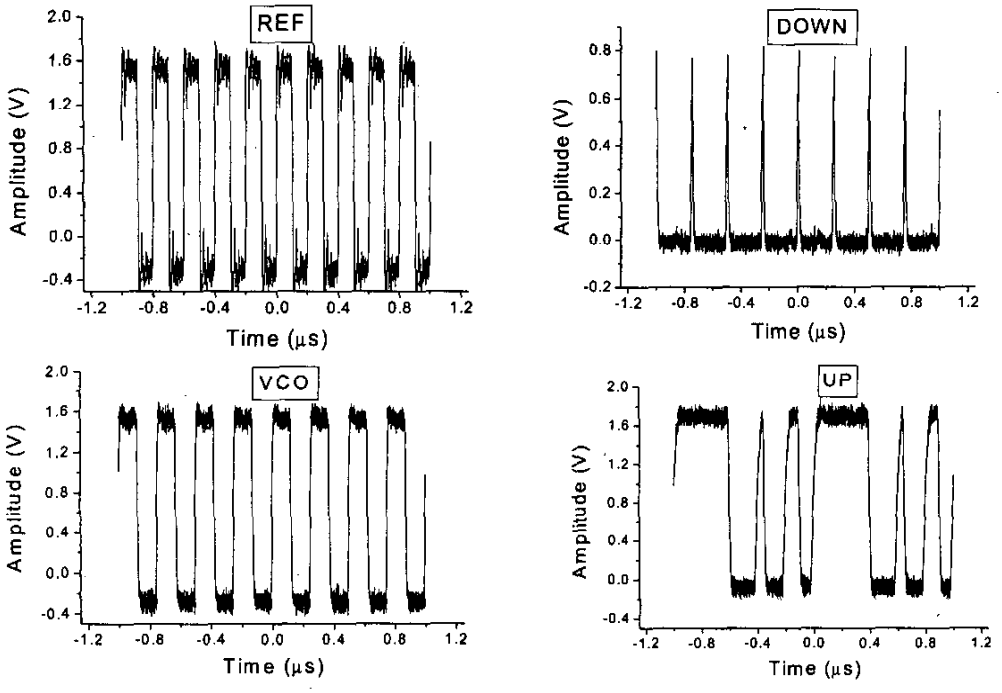

Fig. 5. PFD measurement results when REF = 5 MHz and VCO = 4 MHz

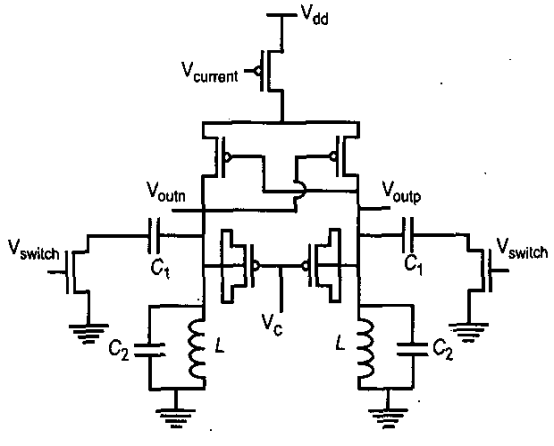

Fig. 7. LC VCO schematic

The RF VCO uses on-chip spiral inductors as part of the LC tank circuit. Fig. 9 shows the equivalent circuit model of the inductor used in the RF VCO along with the quality factor [9]. As can be seen, the quality factor of the inductor is approximately 5.1 over the frequency range of interest.

Fig. 10 shows the phase noise performance of the RF VCO over its tuning range. As can be seen, the frequency range is 1.67-1.89 GHz and has a maximum phase noise of -121 dBc/Hz at an offset of 600 kHz from a carrier of 1.67 GHz.

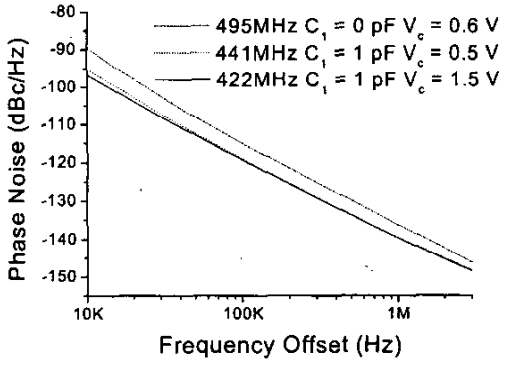

Fig. 8. Phase noise performance of the IF VCO over various frequencies.

VII. PLL Performance Estimation

The total amount of power required for the PLL was estimated to be 36 mW from a 1.8 V supply, with the digital circuitry consuming approximately 1/4 of the total power, the IF VCO 1.3 mW, and the RF VCO 6.54 mW of the total power. The remaining power was consumed by internal buffers in the design.

As shown in the die photo of the IC (Fig. 11) the size of the prototype is 3000 µm x 2000 µm, but can be significantly reduced by eliminating the large number of pads required for testing.

The phase noise performance was found to meet that of the GSM-1800 requirements and the settling time was determined to be 86.15 µs with a loop bandwidth of 1.2 MHz.

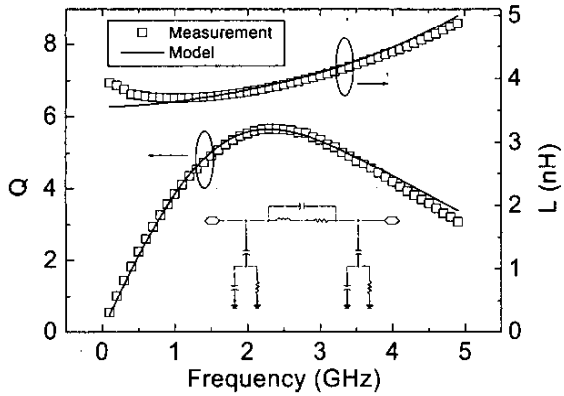

Fig. 9. Equivalent circuit model of the spiral inductor and its quality factor.

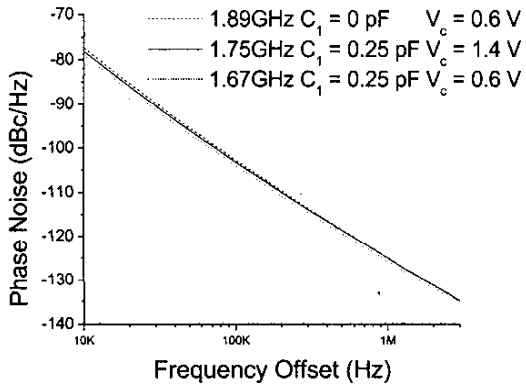

Fig. 10. Phase noise performance of the RF VCO

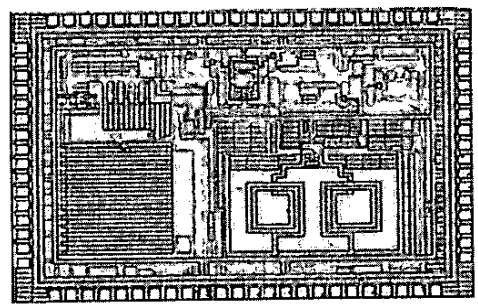

Fig. 11. Die photo of the nested-loop frequency synthesizer

VIII. Conclusions

A fully integrated nested-loop PLL frequency synthesizer for GSM receivers at 1.8 GHz has been presented. The IF VCO operates between 422-495 MHz and the RF VCO operates in the range of 1.67-1.89 GHz. The wide bandwidth nature of this architecture allows for short settling time, while meeting the phase noise requirements for GSM-1800.

ACKNOWLEDGMENTS

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